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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	H. AKIMOTO et al.
Serial No.:	09/975,934
Filed:	October 15, 2001
For:	IMAGE DISPLAY DEVICE (As Amended)
Art Unit:	2674
Examiner:	R. Liang

APPEAL BRIEF

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

November 25, 2002

Sir:

In connection with the above-identified application and further to the amendment after final rejection of August 14, 2002, the Notice of Appeal of September 23, 2002, and the amendment after final rejection of November 25, 2002, which is being submitted herewith, this Appeal Brief is being submitted in triplicate in response to the final Office Action of May 23, 2002, and the Advisory Action of August 20, 2002.

Submitted herewith is a credit card payment form in payment of the fee of $320.00 required for filing this Appeal Brief.

(1) REAL PARTY IN INTEREST

The real party in interest is Hitachi, Ltd., a Japanese corporation, the assignee of the present application. The present application is a continuation of application Serial No. 09/043,534 filed on March 20, 1998, and an assignment assigning all rights in connection with parent application Serial No. 09/043,534 from the inventors to Hitachi, Ltd., was recorded in the U.S. Patent Trademark Office with a recordation date of March 20, 1998, at reel 9418, frame 259.

(2) RELATED APPEALS AND INTERFERENCES

Upon information and belief, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal.

(3) STATUS OF CLAIMS

No claims have been cancelled. Claims 1-15 are pending, with claims 1, 10, and 14-15 being independent. No claims have been allowed. Claims 1-15 have been rejected and are on appeal, and appear in the Appendix attached hereto.

(4) STATUS OF AMENDMENTS

The amendment after final rejection of August 14, 2002, has been entered as indicated in the Advisory Action of August 20, 2002. The amendment after final rejection of August 14, 2002, only amended the section

of the specification entitled "CROSS-REFERENCES TO RELATED APPLICATIONS".

Another amendment after final rejection dated November 25, 2002, is being submitted herewith. The amendment after final rejection of November 25, 2002, also only amends the section of the specification entitled "CROSS-REFERENCES TO RELATED APPLICATIONS". Accordingly, it is presumed that the amendment after final rejection of November 25, 2002, will also be entered.

(5) SUMMARY OF INVENTION

Referring, for example, to Figs. 1-3, the present invention is directed, for example, to an image display which displays image data on an image display part constructed by a display pixel array 18.

An image data input circuit 17, 41, 42, 43, 44, 51, 52 inputs image data into the image display part by selecting addresses in a row direction and a column direction of the display pixel array 18 as shown, for example, in Fig. 2 and described, for example, on page 12, line 12, through page 13, line 5, of the specification so that the display pixel array 18 has two neighboring areas having different frame rates (> 0), such as, for example, the moving picture display area and the still picture display area shown in Fig. 3, as described, for example, on page 13, line 16, through page 15, line 21, and page 16, line 22, through page 17, line 6, of the specification.

The display pixel array 18 includes row direction address lines 50 and column direction address lines 46 as shown, for example, in Fig. 2 and described, for example, on page 9, lines 2-4, of the specification.

Display pixels 47, 48, 49 of the display pixel array 18 each include an AND functional circuit 47 which is connected to one of the row direction address lines 50 and one of the column direction address lines 46 as shown, for example, in Fig. 2 and described, for example, on page 8, line 19, through page 9, line 4, of the specification.

(6) ISSUES

Whether claims 1-15 are properly rejected under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 which issued from parent application Serial No. 09/043,534 of the present application.

(7) GROUPING OF CLAIMS

The claims on appeal stand or fall together because claims 1-15 of the present application are respectively identical to claims 1-9 and 11-16 of U.S. Patent No. 6,329,973, except that the term AND logical circuit in the last paragraph of independent patent claims 1, 11, and 15-16 has been changed to AND functional circuit in independent application claims 1, 10, and 14-15 which respectively correspond to independent patent claims 1, 10, and 15-16, and the only issue is whether the term AND functional circuit in independent application

claims 1, 10, and 14-15 and the term AND logical circuit in independent patent claims 1, 11, and 15-16 have the same scope which is the Examiner's position, or whether these two terms have different scopes, which is the appellants' position.

(8) ARGUMENT

Claims 1-15 were rejected under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 which issued from application Serial No. 09/043,534, the parent application of the present application.

In explaining the rejection, the Examiner states as follows on page 2 of the final Office Action of May 23, 2002:

> Claims 1-15 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-9, 11-16 of prior U.S. Patent No. 6,329,973. This is a double patenting rejection.
>
> The term "AND functional circuit" in the independent claims of the present application and the term "AND logical circuit" in the allowed independent claims of the prior U.S. Patent No. 6,329,973 are directed to the same AND gate circuit, therefore, claims 1-15 of the present application are claiming the same invention as that of claims 1-9, 11-16 of prior U.S. Patent No. 6,329,973.

Claims 1-15 of the present application are respectively identical to claims 1-9 and 11-16 of U.S. Patent No. 6,329,973, except that the term AND logical circuit in the last paragraph of independent patent claims 1, 11, and 15-16 has been changed to AND functional circuit in independent application claims 1, 10,

and 14-15 which respectively correspond to independent patent claims 1, 10, and 15-16.

The Examiner's position that application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 appears to be based on the Examiner's position that the AND functional circuit recited in independent application claims 1, 10, and 14-15 and the AND logical circuit recited in independent patent claims 1, 11, and 15-16 read on AND gate circuit 47 shown, for example, in Fig. 1 and described, for example, on page 8, lines 21-22, of the specification as originally filed.

However, it is submitted that the proper test of whether application claims 1-15 claim the same invention as that of patent claims 1-9 and 11-16 is set forth in MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which provides as follows in pertinent part (emphasis added):

> ***A. Statutory Double Patenting — 35 U.S.C. 101***
>
> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).
>
> A reliable test for double patenting under 35 U.S.C. 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not

> defined by both claims and statutory double patenting would not exist. For example, the invention defined by a claim reciting a compound having a "halogen" substituent is not identical to or substantively the same as a claim reciting the same compound except having a "chlorine" substituent in place of the halogen because "halogen" is broader than "chlorine." On the other hand, claims may be differently worded and still define the same invention. Thus, a claim reciting a widget having a length of "36 inches" defines the same invention as a claim reciting the same widget having a length of "3 feet."

Here, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is broader than the term AND logical circuit recited in independent patent claims 1, 11, and 15-16, such that there are embodiments of the invention which fall within the scope of application claims 1-15 but do not fall within the scope of patent claims 1-9 and 11-16.

For example, it is submitted that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 means any circuit which performs an AND function, while the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 means a logical circuit which performs an AND function.

Attached hereto is a copy of H. Taub et al., Digital Integrated Electronics, 1977, p. 440 (the first page of Chapter 13, "Analog Switches", as indicated on page xiv of the table of contents), McGraw-Hill, New York, ISBN 0-07-062921-8, which states as follows in pertinent part (emphasis added):

> Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level 1 while the other

> range represents logic level **0**. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

In light of this, it is submitted that one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

In contrast, it is submitted that one of ordinary skill in the art would understand that the term AND functional circuit recited in independent application claims 1, 10, and 14-15 is not limited to an implementation with a digital circuit, but means any circuit which performs an AND function, and may be implemented with either a digital circuit, or with an analog circuit, such as, for example, an operational amplifier.

Accordingly, it is submitted that an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application claims 1 and 10, but would arguably not fall within the scope of independent patent claims 1, 11, and 15-16 and dependent application claims 2-9 and 12-14 depending from independent patent claims 1 and 11 because, as discussed above, one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

Accordingly, for the reasons discussed above, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 under the literal infringement test set forth in MPEP 804, such that claims 1-15 of the present application are not properly subject to a double patenting rejection under 35 USC 101 over claims 1-9 and 11-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. patent No. 6,329,973 be reversed.

The above arguments were also presented on pages 4-8 of the amendment of April 25, 2002, and were repeated on pages 3-7 of the amendment of August 14, 2002. In response to these arguments presented in the April 25, 2002, the Examiner states as follows on pages 2-3 of the final Office Action of May 23, 2002 (bold and underlining is the Examiner's):

> Applicant's arguments filed 4/25/2002 have been fully considered but they are not persuasive.
>
> Applicants' remarks regarding the 101 double patenting are not persuasive. The specification **only** discloses an AND gate circuit 47 for performing an AND function and is implemented with a digital circuit, the specification does not disclose or include any analog circuit (such as an operational amplifier) which performs an AND function. Therefore, in light of the specification, both the AND logical circuit in the patented claims and the AND functional circuit in the present claims are directed to the same AND gate circuit 47, there is no any other AND functional circuit

> (for example, analog circuit) to perform the AND function other than the AND gate circuit 47. Therefore, the two recitations are directed to the same circuit and are of the same scope.

With respect to the Examiner's statement that

> The specification **only** discloses an AND gate circuit 47 for performing an AND function and is implemented with a digital circuit . . . .

it is noted that the Examiner has not identified any portion of the specification which supports her position that AND gate 47 in Fig. 1 is implemented with a digital circuit. The Examiner's attention is directed to page 8, line 19, through page 9, line 4, of the specification as amended by the preliminary amendment of October 15, 2001, which reads as follows (emphasis added):

> Each pixel is constructed by a TN liquid crystal capacitor 49, a TFT switch 48 connected to the TN liquid crystal capacitor 49, and an AND gate circuit 47 for driving the gate of the TFT switch 48. The AND gate circuit 47 and the TFT switch 48 are formed by a CMOS process of a poly-Si TFT. The other terminal of the TFT switch 48 is connected to a signal line 45 and input terminals of the AND gate circuit 47 are connected to a vertical direction gate selection line 50 and a horizontal direction gate selection line 46 in the row and column directions, respectively.

and to page 12, line 25, through page 13, line 7, of the specification which reads as follows (emphasis added):

> When an image signal is written in the display pixel, the moving image vertical direction selecting circuit 52 selects an address in the row direction and the moving image horizontal direction selecting circuit 44 selects an address of the moving image in the selected row. As a result, the AND gate circuit 47 of the selected display pixel is turned on and the connected TFT switch 48 is turned on.

It is not seen where anything whatsoever in these passages of the specification or elsewhere in the application supports the Examiner's position that AND gate 47 in Fig. 1 is implemented with a digital circuit.

As the appellants understand it, the Examiner's position is that the term AND functional circuit in the application claims and the term AND logical circuit in the patent claims have the same scope because they both read on AND gate circuit 47 in Fig. 2 which is the only AND circuit disclosed in the application. However, the Examiner has not cited any basis whatsoever in the statutes, rules, procedures, and decisions in support of her position, and it is submitted that the position taken by the Examiner is improper and contrary to law because the test for a statutory double patenting rejection under 35 USC 101 is not whether terms in two claims read on the same element in the disclosure as in the Examiner' position, but whether the terms in the two claims have different scopes under the literal infringement test set forth in the pertinent part of MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which is reproduced above.

For example, assume that an application discloses a circuit including a MOSFET transistor which is the only transistor disclosed in the application, and that the application issues as a patent with claims specifically reciting a MOSFET transistor. Before the application issues as a patent, a continuation application is filed presenting claims which are identical to the claims of the patent except that the application claims recite a transistor, rather than a MOSFET transistor as recited in the patent claims.

It is submitted that the application claims reciting a transistor are broader than the patent claims reciting a MOSFET transistor because an embodiment of the invention including a bipolar junction transistor would literally infringe the application claims reciting a transistor but would not literally infringe the patent claims reciting a MOSFET transistor, such that the application claims and the patent claims would not be defining identical subject matter and statutory double patenting under 35 USC 101 would not exist between the application claims and the patent claims under the literal infringement test set forth in the pertinent part of MPEP 804, Eighth Edition, August 2001, pp. 800-20 to 800-21, which is reproduced above.

Similarly, it is submitted that the term AND functional circuit in the claims of the present application and the term AND logical circuit in the claims of U.S. Patent No. 6,329,973 do in fact have different scopes for the reasons discussed in detail above, i.e. because an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application claims 1 and 10, but would arguably not fall within the scope of independent patent claims 1, 11, and 15-16 and dependent application claims 2-9 and 12-14 depending from independent patent claims 1 and 11 because, as discussed above, one of ordinary skill in the art might arguably interpret the term AND logical circuit recited in independent patent claims 1, 11, and 15-16 to mean a logical circuit which performs an AND function and is implemented with a digital circuit.

Accordingly, for the reasons discussed above, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 under the literal infringement test set forth in MPEP 804, such that claims 1-15 of the present application are not properly subject to a double patenting rejection under 35 USC 101 over claims 1-9 and 11-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. patent No. 6,329,973 be reversed.

The above arguments were also presented on pages 7-11 of the amendment of August 14, 2002. In response to these arguments, the Examiner states as follows in the Advisory Action of August 20, 2002:

> 5. The c) the remarks has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
>
> . . . .
>
> Continuation of 5. does NOT place the application in condition for allowance because: the examiner disagrees with applicant's argument, see previous Office Action [the final Office Action of May 23, 2002]..

However, the arguments presented on pages 7-11 of the amendment of August 14, 2002, which are reproduced above were newly presented in the amendment of August 14, 2002, and explained why the Examiner's position set

forth in the "previous Office Action" [the final Office Action of May 23, 2002] is improper.

Accordingly, it is submitted that the Examiner's mere reference to the "previous Office Action [the final Office Action of May 23, 2002]" in the Advisory Action of August 20, 2002, cannot serve to rebut the newly presented arguments on pages 7-11 of the amendment of August 14, 2002, because this mere reference does not take note of the newly presented arguments on pages 7-11 of the amendment of August 14, 2002, and answer the substance of them as required by MPEP 707.07(f), Eighth Edition, August 2001, page 700-98, which provides as follows in pertinent part (emphasis added):

> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.

Accordingly, for the reasons discussed above, it is submitted that claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 under the literal infringement test set forth in MPEP 804, such that claims 1-15 of the present application are not properly subject to a double patenting rejection under 35 USC 101 over claims 1-9 and 11-16 of U.S. Patent No. 6,329,973.

Since claims 1-15 of the present application do not claim the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 for the reasons discussed above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. patent No. 6,329,973 be reversed.

CONCLUSION

For the reasons set forth above, it is respectfully requested that the rejection of claims 1-15 under 35 USC 101 as claiming the same invention as that of claims 1-9 and 11-16 of U.S. Patent No. 6,329,973 be reversed.

To the extent necessary, the appellants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees and appeal fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.36114CX1).

Respectfully submitted,

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Attachments

APPENDIX

1. An image display which displays image data on an image display part constructed by a display pixel array, wherein an image data input circuit inputs image data into the image display part by selecting addresses in a row direction and a column direction of the display pixel array so that the display pixel array has two neighboring areas having different frame rates (> 0);

wherein the display pixel array includes row direction address lines and column direction address lines; and

wherein display pixels of the display pixel array each include an AND functional circuit which is connected to one of the row direction address lines and one of the column direction address lines.

2. An image display according to claim 1, further comprising:

an image data generating circuit; and

a signal transmitting circuit which wirelessly transmits image data generated by the image data generating circuit to the image data input circuit.

3. An image display according to claim 2, further comprising:

a second image display part having a smaller portability than the image display part; and

a second signal transmitting circuit which transmits over a wire image data generated by the image data generating circuit to the second image display part.

4. An image display according to claim 1, further comprising a frame rate selecting circuit which selects a frame rate of the display pixel array on a display pixel unit basis.

5. An image display according to claim 1, wherein the image data input circuit inputs image data having a first gradation precision into one area of the display pixel array, and inputs image data having a second gradation precision which is different from the first gradation precision into another area of the display pixel array.

6. An image display according to claim 5, wherein the image data input circuit inputs image data having only two gradations into the one area of the display pixel array.

7. An image display according to claim 1, wherein the image data is divided into frames; and

wherein the image data input circuit divides each of the frames of the image data into a first number of fields when inputting image data into one area of the display pixel array, and divides each of the frames of the image data

into a second number of fields which is different from the first number of fields when inputting image data into another area of the display pixel array.

8. An image display according to claim 1, wherein when a shape or a position of an area of the display pixel array into which image data is being inputted at a first frame rate which is different from a second frame rate at which image data is being inputted into another area of the display pixel array changes, the image data input circuit preferentially inputs image data into the area of the display pixel array having the changed shape or position.

9. An image display according to claim 1, wherein the display pixel array is a liquid crystal display pixel array using a TN (Twisted Nematic) mode liquid crystal.

10. An image display which displays image data on an image display part constructed by a display pixel array, wherein an image data input circuit inputs at least one moving image data and at least one still image data at different frame rates (> 0) into the image display part by selecting addresses in a row direction and a column direction of the display pixel array;

wherein the display pixel array includes row direction address lines and column direction address lines; and

wherein display pixels of the display pixel array each include an AND functional circuit which is connected to one of the row direction address lines and one of the column direction address lines.

11. An image display according to claim 10, wherein the moving image data is inputted into the image display part in a real-time manner from generation of data.

12. An image display according to claim 10, further comprising a still image data storing circuit which temporarily stores the still image data until it is inputted into the image display part.

13. An image display according to claim 12, further comprising a code data storing circuit which temporarily stores two-gradation text and figure data in a predetermined code data format until it is inputted into the image display part.

14. An image display which displays image data on an image display part constructed by a display pixel array, wherein image data input means inputs image data into the image display part by selecting addresses in a row direction and a column direction of the display pixel array so that the display pixel array has two neighboring areas having different frame rates (> 0);

wherein the display pixel array includes row direction address lines and column direction address lines; and

wherein display pixels of the display pixel array each include an AND functional circuit which is connected to one of the row direction address lines and one of the column direction address lines.

15. An image display which displays image data on an image display part constructed by a display pixel array, wherein image data input means inputs at least one moving image data and at least one still image data at different frame rates (> 0) into the image display part by selecting addresses in a row direction and a column direction of the display pixel array;

wherein the display pixel array includes row direction address lines and column direction address lines; and

wherein display pixels of the display pixel array each include an AND functional circuit which is connected to one of the row direction address lines and one of the column direction address lines.

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13

ANALOG SWITCHES

Digital waveforms, ideally at least, make abrupt transitions between two separated ranges of values. One range represents logic level **1** while the other range represents logic level **0**. Within each range, the exact signal level is of no significance. In logical gates all inputs and outputs are digital signals.

Analog voltages, on the other hand, are voltages whose precise value is always significant. Such analog voltages may be fixed in value or may make excursions through a continuous range of values. There frequently occurs a need for switches in circuits and systems involving analog signals, in which the opening and closing of the switches are to be controlled by digital waveforms. Circuits of this type are variously called *analog gates*, *transmission gates*, *linear gates*, *time-selection circuits*, etc., depending on the purpose to which the circuit is put. The switch-control digital waveform is referred to as the *gating signal*, the *control signal*, or the *logic input*.